NEPAL ENGINEERING COUNCIL (NEC)

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REGISTRATION EXAMINATION FOR COMPUTER ENGINEERING (BCT) — MODEL EXAM SET 02

Time Allowed:	Maximum Marks:	Pass Marks:	Negative Marking:
2 Hours (120 Mins)	**100 Marks**	**50 Marks**	**Nil (None)**

Candidate Name: ..... Roll No: ..... Center: .....

INSTRUCTIONS TO CANDIDATES

1. This Question Booklet contains **100 Multiple Choice Questions (MCQs)** derived strictly from the official NEC Model Sets, Mock Examinations, and Sanfoundry curriculum across all 10 chapters of the official NEC Computer Engineering (ACtE) Syllabus.
2. Each question carries **1 (one) mark**. All questions are compulsory. There is **no negative marking**.
3. Each question has four options marked (A), (B), (C), and (D). Select only **ONE** best answer for each question.
4. Darken the corresponding oval completely on the Optical Mark Recognition (OMR) Answer Sheet with a black or blue ballpoint pen.
5. Non-programmable scientific calculators are permitted. Electronic storage devices, smart watches, and mobile phones are strictly prohibited.

SECTION I: CONCEPT OF BASIC ELECTRICAL AND ELECTRONICS ENGINEERING

Questions 01 – 10 (10 Marks)

Q.01 1.1 Basic Concept: Decibel Power Gain

Decibel relation for power gain is given by:

(A) $N_{dB} = 20\log_{10}\left(\frac{V_2^2}{V_1^2}\right) + 20\log_{10}\left(\frac{Z_1}{Z_2}\right)$

(B) $N_{dB} = 10\log_{10}\left(\frac{V_2^2}{V_1^2}\right) + 10\log_{10}\left(\frac{Z_1}{Z_2}\right)$

(C) $N_{dB} = 20\log_{10}\left(\frac{V_2}{V_1}\right) + 10\log_{10}\left(\frac{Z_2}{Z_1}\right)$

(D) $N_{dB} = 10\log_{10}\left(\frac{V_2}{V_1}\right) + 10\log_{10}\left(\frac{Z_2}{Z_1}\right)$

Q.02 1.2 Network Theorems: Maximum Power Transfer

Maximum power that can be transferred from an electrical source to a variable load is:

(A) 25%
(B) 75%
(C) 50%
(D) 100%

Q.03 1.2 AC Circuits: Power Factor

In an AC electrical circuit, the power factor (R/Z) has a maximum theoretical value of:

(A) 0.0
(B) 0.5
(C) 1.0
(D) 1.5

Q.04 1.4 Semiconductor Devices: EEPROM Physics

In an EEPROM (Electrically Erasable Programmable Read-Only Memory) cell, the tunnel oxide gap between the drain and the floating gate is approximately:

(A) 5 nm
(B) 10 nm
(C) 15 nm
(D) 20 nm

Q.05 1.4 Semiconductor Physics: Quantum Principles

The Heisenberg Uncertainty Principle states that the product of uncertainty in position (Δx) and uncertainty in momentum (Δp) satisfies:

(A) $\Delta x \cdot \Delta p \geq \frac{h}{4\pi}$
(B) $\Delta x \cdot \Delta p \leq \frac{h}{4\pi}$
(C) $\Delta x \cdot \Delta p = \frac{h}{4\pi}$
(D) None of the above

Q.06 1.6 Amplifiers & Output Stages: Microwave Amplification

An Ultra High Frequency (UHF: 300 MHz – 3 GHz) signal can be amplified using which of the following vacuum tube devices?

(A) Klystron tube
(B) Magnetron
(C) Traveling Wave Tube (TWT)
(D) All of the above

Q.07 1.2 R-L-C Circuits: Q-Factor Calculation

A $10\ \mu\text{H}$ inductor, a $40\ \text{pF}$ capacitor, and a $628\ \Omega$ resistor are connected to form a series RLC circuit. What is the Q-factor of this circuit at its resonant frequency?

(A) 1.0142×10^{-6}
(B) 2.50
(C) 1.0142×10^{-9}
(D) 2.50×10^{-3}

Q.08 1.3 Alternating Current Fundamentals: Inductive Reactance

A $400\ \text{mH}$ coil of negligible resistance is connected to an AC circuit in which an effective RMS current of $6\ \text{mA}$ is flowing. Find the voltage across the coil if the supply frequency is $1000\ \text{Hz}$:

(A) 15.07 V
(B) 15079.67 V
(C) 150.79 V
(D) 15079 V

Q.09 1.3 AC Fundamentals: Pure Resistive Circuit

For a purely resistive AC circuit, what is the phase angle between the applied alternating voltage and the resulting alternating current?

(A) 90°
(B) 0°
(C) 180°
(D) 45°

Q.10 1.4 Semiconductor Devices: Diodes

What is the primary function of a semiconductor diode in power conversion circuits?

(A) Amplification
(B) Rectification
(C) Modulation
(D) Oscillation

SECTION II: DIGITAL LOGIC AND MICROPROCESSOR

Questions 11 – 20 (10 Marks)

Q.11 2.1 Number Systems: 2's Complement

The two's complement of binary number `00011011` is:

(A) `11100100`
(B) `11100101`
(C) `11000101`
(D) `11101001`

Q.12 2.2 Combinational Logic: Building Blocks

The elementary building block of a combinational logic circuit is:

(A) Logic Gate
(B) Flip-Flop
(C) Both Logic Gate and Flip-Flop
(D) None of the above

Q.13 2.3 Sequential Logic: Clocked Circuits

A synchronous sequential circuit that changes its internal binary state at a specific clock edge or signal transition is called a:

(A) Flip-Flop
(B) Latch
(C) Multiplexer
(D) Decoder

Q.14 2.4 Microprocessor Architecture: Bus Width

The bandwidth (bus capability) of a microprocessor fundamentally represents its:

(A) Word size only
(B) Clock speed only
(C) Number of data lines (Data bus width)
(D) Address bus width

Q.15 2.5 Microprocessor Systems: Intel 8255 PPI

The Intel 8255 Programmable Peripheral Interface (PPI) chip has an internal data bus of size:

(A) 8 bit
(B) 16 bit
(C) 32 bit
(D) 64 bit

Q.16 2.6 Interrupt Operations: ISR Execution

An Interrupt Service Routine (ISR) executes:

(A) Before the interrupt request is acknowledged
(B) In response to (during the servicing of) an accepted interrupt request
(C) Only after the main program has fully terminated
(D) None of the above

Q.17 2.1 Number Systems: Octal to Decimal Conversion

Convert the octal number $(312)_8$ into its equivalent decimal representation:

(A) 200
(B) 202
(C) 204
(D) 206

Q.18 2.4 Embedded Controllers: Timer Clock Calculations

A microcontroller executes a program with a master clock frequency of $8\ \text{MHz}$. If a hardware timer requires 250 clock cycles to trigger an interrupt, what is the exact time interval between successive interrupts?

(A) $31.25\ \mu\text{s}$

(B) $31.25\ \text{ms}$

(C) $125\ \mu\text{s}$

(D) $250\ \mu\text{s}$

Q.19 2.3 Sequential Logic: Latches

In an active-low cross-coupled NAND $\bar{S}$-$\bar{R}$ latch, which input combination is invalid / forbidden because it causes both outputs to become HIGH simultaneously?

(A) $\bar{S} = 1, \bar{R} = 1$

(B) $\bar{S} = 0, \bar{R} = 1$

(C) $\bar{S} = 1, \bar{R} = 0$

(D) $\bar{S} = 0, \bar{R} = 0$

Q.20 2.4 Microprocessor: Instruction Timing

In the Intel 8085 microprocessor, how many machine cycles and T-states are required to execute the 3-byte instruction `STA 2050H`?

(A) 3 machine cycles, 10 T-states

(B) 4 machine cycles, 13 T-states

(C) 2 machine cycles, 7 T-states

(D) 5 machine cycles, 16 T-states

SECTION III: PROGRAMMING LANGUAGE AND ITS APPLICATIONS

Questions 21 – 30 (10 Marks)

Q.21 3.1 C Programming: Standard I/O

What is the primary function and purpose of the `printf()` function in the C standard library (`stdio.h`)?

(A) To read formatted input characters from the standard input keyboard buffer

(B) To declare variable types and assign dynamic stack memory

(C) To write formatted characters, text, and numerical variables to the standard output stream (`stdout`)

(D) To perform mathematical floating-point rounding

Q.22 3.2 Data Files in C: File Pointer Control

What is the purpose of the `rewind()` function in C programming file handling?

(A) To reset the file position indicator to the very beginning (offset 0) of the specified file stream

(B) To permanently delete the file contents from disk storage

(C) To reverse the order of bytes inside the file

(D) To close an active file handle and flush disk buffers

Q.23 3.3 C++ Classes & Objects: Access Specifiers

Which access specifier in C++ allows member variables and member functions to be accessed strictly and exclusively within member functions and friend classes of the same class?

(A) `package`

(B) `private`

(C) `public`

(D) `protected`

Q.24 3.3 Constructors and Destructors in C++

What is the primary architectural purpose of a **Constructor in C++?**

(A) To deallocate heap memory when an object goes out of scope

(B) To prevent the class from being derived or inherited

(C) To override virtual functions at runtime

(D) To initialize the member variables and acquire resources for an object automatically upon its creation

Q.25 3.5 Pure Virtual Functions & Abstract Classes

Which of the following statements regarding **Pure Virtual Functions in C++ is strictly TRUE?**

(A) Pure virtual functions cannot be overridden by concrete derived classes

(B) Pure virtual functions can only accept `void` argument lists

(C) A class declaring at least one pure virtual function becomes an abstract class and cannot be directly instantiated

(D) A pure virtual function must always provide a non-empty implementation in the base class

Q.26 3.6 Exception Handling Constructs

In C++ exception handling, what is the role of the `try` block?

(A) To enclose a block of statements that might potentially throw an exception during execution

(B) To declare global error logging handlers

(C) To catch and handle specific runtime error objects

(D) To force execution termination if an error condition is encountered

Q.27 3.2 Pointers in C: Dereferencing and Modification

What is the terminal output of the following C program segment?

```
 int x = 10;
int *p = &x;
*p += 5;
printf("%d", x);
```

(A) 10

(B) Address of x

(C) Garbage value

(D) 15

Q.28 3.3 C++ Functions: Default Arguments

In C++, where must default arguments be placed in a function declaration's parameter list?

(A) Anywhere in the parameter list in any arbitrary order

(B) Trailing at the right-hand end of the parameter list (all parameters to the right of a default argument must also have defaults)

(C) Only for pointer and reference parameters

(D) Only at the beginning of the parameter list

Q.29 3.6 Exception Handling Keywords

Which C++ keyword is used to raise (throw) an exception when an abnormal condition is detected?

(A) `throws`

(B) `catch`

(C) `throw`

(D) `try`

Q.30 3.2 Pointers and Arrays in C

Which of the following statements regarding the relationship between pointers and arrays in C is TRUE?

(A) An array name evaluates to a constant pointer pointing to its first element: `arr == &arr[0]`

(B) An array name is a modifiable l-value pointer variable that can be assigned a new address

(C) Pointers cannot be accessed using array subscript notation `[]`

(D) `sizeof(arr)` for `int arr[10]` evaluates to the size of a pointer (8 bytes on 64-bit OS)

SECTION IV: COMPUTER ORGANIZATION AND EMBEDDED SYSTEM

Questions 31 – 40 (10 Marks)

Q.31 4.1 CPU Architecture: Addressing Modes

Which of the following is NOT a standard CPU instruction addressing mode?

(A) Immediate addressing

(B) Direct addressing

(C) Relative addressing

(D) Virtual addressing

Q.32 4.2 Memory Hierarchy: Cache Memory Principles

Which fundamental principle of computer program execution forms the foundation for cache memory design and hierarchy?

(A) Principle of Locality (Temporal and Spatial Locality)

(B) Von Neumann bottleneck principle

(C) Amdahl's law of parallel speedup

(D) Moore's law of transistor scaling

Q.33 4.3 Multiprocessor Systems: Characteristics

Which of the following is NOT a typical characteristic of a multiprocessor computing system?

(A) Enhanced system reliability through redundancy and fault tolerance

(B) Increased throughput and compute performance via concurrent task execution

(C) Completely isolated execution with zero shared memory, shared peripherals, or inter-processor communication

(D) Resource and memory sharing among cooperating processors

Q.34 4.4 Embedded Systems: ASIP

What is an Application-Specific Instruction-Set Processor (ASIP)?

(A) A standard off-the-shelf general-purpose CPU like an Intel Core i7

(B) A processor whose architecture and instruction set are customized and optimized for a specific application domain

(C) An analog processing circuit without registers

(D) A fixed-function ASIC without an instruction decoder

Q.35 4.5 Real-Time Embedded Systems: Watchdog Timers

What is the primary operational role of a **Watchdog Timer in an embedded Real-Time Operating System (RTOS)?**

(A) To measure dynamic processor power consumption

(B) To detect software lockups or crashes and automatically reset the system to recover safe operation

(C) To synchronize the system calendar clock with network NTP time servers

(D) To prioritize thread scheduling in the ready queue

Q.36 4.6 Hardware Description Languages: VHDL

In digital electronics and ASIC/FPGA design, what does the acronym **VHDL stand for?**

(A) Very High Density Logic

(B) VHSIC (Very High Speed Integrated Circuit) Hardware Description Language

(C) Virtual Hardware Definition Language

(D) Verified Hardware Development Layout

Q.37 4.3 I/O Organization: Direct Memory Access (DMA)

Which mode of I/O data transfer enables high-speed peripheral devices to transfer data blocks directly to and from system memory without continuous intervention from the CPU?

(A) Programmed I/O

(B) Interrupt-Driven I/O

(C) Direct Memory Access (DMA)

(D) Polled I/O

Q.38 4.5 Operating Systems: RTOS vs GPOS

What is the primary operational difference between a Real-Time Operating System (RTOS) and a General-Purpose Operating System (GPOS)?

(A) An RTOS provides deterministic timing guarantees ensuring tasks complete within strict deadlines, whereas a GPOS prioritizes overall average throughput

(B) An RTOS supports multi-threading, whereas a GPOS supports only single-threaded execution

(C) An RTOS requires significantly more RAM and disk storage than a GPOS

(D) An RTOS cannot service hardware interrupts

Q.39 4.2 Memory Hierarchy: Latency

In the standard computer memory hierarchy, which memory layer is physically located closest to the CPU execution units and offers the lowest latency access?

(A) Main Memory (DRAM)

(B) L1 Cache (SRAM)

(C) Solid-State Storage (NVMe Flash)

(D) Hard Disk Drive (Magnetic Storage)

Q.40 4.1 Processor Architecture: RISC vs CISC

Which of the following architectural characteristics is a defining feature of Reduced Instruction Set Computers (RISC)?

(A) Variable-length complex instructions with many memory addressing modes

(B) Simple, fixed-length instructions executed mostly in a single clock cycle with a load/store memory model

(C) Microprogrammed control units storing microinstructions in control ROM

(D) Absence of general-purpose register files

SECTION V: CONCEPT OF COMPUTER NETWORK AND NETWORK SECURITY SYSTEM

Questions 41 – 50 (10 Marks)

Q.41 5.1 Physical and Data Link Devices: Switches

Which networking device operates primarily at the Data Link layer (Layer 2) of the OSI model and forwards traffic based on MAC addresses?

(A) Network Switch / Bridge

(B) Hub

(C) Router

(D) Gateway

Q.42 5.2 Data Link Layer: Error Detection

Which error detection technique involves dividing the data bit stream by a predetermined generator polynomial using modulo-2 arithmetic and appending the remainder as check bits?

(A) Internet Checksum
(B) Hamming Code
(C) Cyclic Redundancy Check (CRC)
(D) Simple Parity check

Q.43 5.3 Network Layer: Routing Protocols

Which graph routing algorithm is employed by the Open Shortest Path First (OSPF) routing protocol to calculate the best route to all destinations?

(A) Distance Vector algorithm
(B) Dijkstra's Shortest Path First (SPF) algorithm
(C) Bellman-Ford algorithm
(D) Floyd-Warshall all-pairs algorithm

Q.44 5.4 Transport Layer: Protocols

Which protocol at the transport layer of the Internet protocol suite provides reliable, connection-oriented, full-duplex byte-stream delivery with flow and congestion control?

(A) User Datagram Protocol (UDP)
(B) Internet Control Message Protocol (ICMP)
(C) Address Resolution Protocol (ARP)
(D) Transmission Control Protocol (TCP)

Q.45 5.5 Application Layer: Protocols

Which application layer protocol is standardly used for transmitting and relaying electronic mail between mail servers?

(A) SMTP (Simple Mail Transfer Protocol)
(B) IMAP (Internet Message Access Protocol)
(C) HTTP (Hypertext Transfer Protocol)
(D) POP3 (Post Office Protocol v3)

Q.46 5.6 Network Security: Firewalls

Which network security device or software subsystem monitors and controls incoming and outgoing network traffic based on predetermined security rules?

(A) Modem
(B) Router
(C) Firewall
(D) Hub

Q.47 5.2 Data Link & Network Layers: ARP

What is the primary function of the Address Resolution Protocol (ARP) in IPv4 local area networks?

(A) To resolve human-readable domain names into 32-bit IP addresses
(B) To automatically assign dynamic IP addresses, default gateways, and DNS servers to client devices
(C) To translate private IPv4 addresses into public IP addresses
(D) To dynamically resolve a known Layer 3 IPv4 address into its corresponding Layer 2 physical MAC address

Q.48 5.3 Network Layer: Diagnostic Protocols

Which Network layer protocol is used by network devices (such as routers and hosts) to send error messages and operational information regarding network connectivity (e.g. Destination Unreachable, TTL Expired)?

(A) ARP
(B) ICMP
(C) RARP
(D) IGMP

Q.49 5.5 Application Layer: DNS Port

What is the standard well-known transport port number used by the Domain Name System (DNS) for routine name query resolution?

(A) Port 443
(B) Port 25
(C) Port 53
(D) Port 80

Q.50 5.6 Network Security: Asymmetric Cryptography

In public-key asymmetric cryptography (such as RSA), which key must the sender use to encrypt a confidential message so that ONLY the intended recipient can read it?

(A) Recipient's public key
(B) Sender's private key
(C) Sender's public key
(D) Recipient's private key

SECTION VI: THEORY OF COMPUTATION AND COMPUTER GRAPHICS

Questions 51 – 60 (10 Marks)

Q.51 6.5 2D Viewing & Line Clipping: Cohen-Sutherland

What is the foundational concept behind the Cohen-Sutherland line clipping algorithm?

(A) Parametric vector equations of lines
(B) Recursive binary subdivision of line segments
(C) Polygon edge intersection winding numbers
(D) Dividing the 2D plane into 9 regions and assigning 4-bit region outcodes to classify endpoints

Q.52 6.5 2D Viewing & Line Clipping: Outcodes

The region outcode assigned to endpoints in the Cohen-Sutherland line clipping algorithm consists of how many bits?

(A) 8 bits
(B) 4 bits
(C) 16 bits
(D) 2 bits

Q.53 6.5 2D Viewing: Trivial Rejection

In the Cohen-Sutherland algorithm, which bitwise logical operation on the endpoint region codes determines whether a line segment lies completely outside the clipping window (trivial rejection)?

(A) Bit Shift
(B) Logical XOR
(C) Logical AND
(D) Logical OR

Q.54 6.5 2D Viewing: Trivial Acceptance

In the Cohen-Sutherland algorithm, a line segment is completely accepted (drawn in its entirety without clipping) if:

(A) The region codes of both endpoints are strictly zero (`0000`)
(B) Both region codes are non-zero
(C) The logical AND of region codes is non-zero
(D) The logical OR of region codes is non-zero

Q.55 6.5 2D Line Clipping: Liang-Barsky Advantages

What is the primary computational advantage of the Liang-Barsky line clipping algorithm compared to the Cohen-Sutherland algorithm?

(A) It does not require viewport bounding coordinates
(B) It completely eliminates the parameter t
(C) It avoids all geometric calculations
(D) It uses parametric equations of lines, resulting in significantly fewer intersection calculations and fewer floating-point operations

Q.56 6.5 2D Line Clipping: Liang-Barsky Equations

In the Liang-Barsky line clipping algorithm, what is the parametric mathematical equation representing a 2D line segment between endpoints (x_1, y_1) and (x_2, y_2) for parameter $0 \leq t \leq 1$?

(A) $x = x_1 + t(x_2 - x_1), \quad y = y_1 + t(y_2 - y_1)$

(B) $x = (1-t)x_1 + tx_2, \quad y = (1-t)y_1 + ty_2$

(C) $x = x_{min} + t(x_2 - x_1), \quad y = y_{min} + t(y_2 - y_1)$

(D) $x = t(x_1 - x_2) + x_2, \quad y = t(y_1 - y_2) + y_2$

Q.57 6.1 Finite Automata: Determinism

What is the defining mathematical property of a Deterministic Finite Automaton (DFA) regarding its transition function $\delta(q, a)$?

(A) For each state and input symbol, there may be zero, one, or multiple next states

(B) Transitions may occur spontaneously without consuming an input symbol (ϵ-transitions)

(C) For each state and input symbol, there is exactly one unique transition to a next state

(D) The automaton possesses an unbounded external pushdown stack

Q.58 6.3 Turing Machines: Model Definition

Which theoretical computational machine model consists of a finite-state control unit coupled with an infinitely long, bidirectional read/write tape?

(A) Pushdown Automaton (PDA)

(B) Turing Machine (TM)

(C) Linear Bounded Automaton (LBA)

(D) Finite State Automaton (FSA)

Q.59 6.2 Context-Free Grammars: Chomsky Normal Form

A Context-Free Grammar (CFG) is in Chomsky Normal Form (CNF) if every production rule is strictly of the form:

(A) $A \to BC \quad \text{or} \quad A \to a$

(B) $A \to BCD$

(C) $A \to aB \quad \text{or} \quad A \to a$

(D) $A \to \alpha B \beta$

Q.60 6.4 Computer Graphics: Line Drawing Algorithms

Which line drawing algorithm utilizes an incremental integer decision parameter to determine the next pixel position, completely eliminating floating-point multiplications, divisions, and rounding operations?

(A) Digital Differential Analyzer (DDA)

(B) Midpoint Circle Algorithm

(C) Cohen-Sutherland Algorithm

(D) Bresenham's Line Algorithm

SECTION VII: DATA STRUCTURES, DATABASE SYSTEM AND OPERATING SYSTEM

Questions 61 – 70 (10 Marks)

Q.61 7.3 Database Architecture: Schema Levels

In the standard ANSI/SPARC 3-level database architecture, at which level does the model describe the physical data structures, storage allocation, and file indexing to produce an executable, compatible database on disk?

(A) Conceptual Level

(B) External (View) Level

(C) Internal (Physical) Level

(D) Logical Level

Q.62 7.2 Searching & Hashing: Division Method

In hash table addressing, what is the mathematical hash function used in the standard **Division Method of hashing for integer key k and table size m?**

(A) $h(k) = k \bmod m$

(B) $h(k) = \lfloor m(kA \bmod 1) \rfloor$

(C) $h(k) = (k + m) \bmod 2$

(D) $h(k) = k/m$

Q.63 7.3 Database Normalization: Purpose

Data redundancy, update anomalies, insertion anomalies, and deletion anomalies are systematically eliminated from relational database tables using the process of:

(A) Data Aggregation

(B) Denormalization

(C) Table Indexing

(D) Normalization (Normal Forms)

Q.64 7.4 Database Transactions: Crash Recovery

In database crash recovery systems implementing Write-Ahead Logging (WAL), it is mandatory to write and flush the _____ to stable non-volatile storage before the actual modified data page is written to disk.

(A) Database Schema Definition

(B) Transaction Log record

(C) B-Tree Index File

(D) User Session Cookie

Q.65 7.5 Operating Systems: Process Concurrency

In operating system process synchronization, to enforce mutual exclusion around a critical region, two standard functions are required: `enter_critical()` and:

(A) `exit_critical()`

(B) `abort()`

(C) `terminate()`

(D) `wait()`

Q.66 7.6 System Administration: User Access Control

In operating system security and system administration, what mechanism ensures that only authorized administrators can execute privileged system configuration commands?

(A) Spooling daemon redirection

(B) Virtual memory demand paging

(C) Privileged user role authentication (e.g. `sudo` / Administrator account password authentication)

(D) CPU burst time scheduling

Q.67 7.1 Data Structures: Linked List Recursion

What is the behavior and output of the following recursive C function when passed the pointer to the head of a singly linked list?

```
void fun(struct Node* head) {
    if (head == NULL) return;
    fun(head->next);
    printf("%d ", head->data);
}
```

(A) Prints the elements of the linked list in their forward sequential order

(B) Deletes all nodes in the linked list recursively

(C) Calculates the total number of nodes in the linked list

(D) Prints the elements of the linked list in reverse order (from tail to head)

Q.68 7.5 Operating Systems: FCFS Scheduling Calculation

Three processes P_1, P_2, P_3 arrive simultaneously at time $t = 0$ ms with CPU burst times of 24 ms, 3 ms, 3 ms, respectively. Under First-Come First-Served (FCFS) scheduling in the order P_1, P_2, P_3, what is the average waiting time?

(A) 30 ms
(B) 17 ms
(C) 13 ms
(D) 27 ms

Q.69 7.1 Data Structures: Binary Heap

In a binary Max-Heap containing n elements, where is the element with the maximum key value guaranteed to reside?

(A) At the root node (index 0 or 1)
(B) At index $\lfloor n/2 \rfloor$
(C) In the leftmost leaf node
(D) In the rightmost leaf node

Q.70 7.1 Data Structures: Stack Applications

Which fundamental data structure operates strictly on the Last-In First-Out (LIFO) discipline and is the standard implementation choice for matching nested parentheses in compiler syntax parsing?

(A) Queue
(B) Priority Queue
(C) Circular Linked List
(D) Stack

SECTION VIII: SOFTWARE ENGINEERING AND OOAD

Questions 71 – 80 (10 Marks)

Q.71 8.1 Requirements Engineering: Process Definition

The disciplined engineering process to elicit software requirements from clients/users, analyze, specify, validate, and document them into a formal SRS is known as:

(A) Requirement Engineering
(B) Software Prototyping
(C) Software Testing
(D) Reverse Engineering

Q.72 8.2 Software Design: Reference Architecture

In software architecture and system design, what is a **Reference Architecture?**

(A) A temporary UML activity diagram drawn during initial brainstorming
(B) A binary compiler intermediate representation
(C) A generalized, proven architectural template providing standard structures and best-practice solutions for a specific application domain
(D) A physical server rack wiring diagram

Q.73 8.4 OOAD: Access Visibility

Which access visibility specifier in object-oriented design makes members accessible within the declaring class and its derived sub-classes, but protects them from direct external client access?

(A) `default`
(B) `protected`
(C) `public`
(D) `private`

Q.74 8.6 Object-Oriented Implementation: Operator Overloading

In object-oriented programming (such as C++), what is **Operator Overloading?**

(A) Overwriting machine assembly instructions in memory
(B) Converting all binary operators into unary operators
(C) Restricting arithmetic operations in code
(D) Redefining the behavior of existing language operators (e.g. `+`, `==`, `<<`) to perform user-defined operations on custom class objects

Q.75 8.6 OO Implementation: C++ Streams

In the C++ Standard Stream Library (`<fstream>`), what is the functional difference between `ifstream` and `ofstream` ?

(A) Both streams are used exclusively for console standard input

(B) `ifstream` is used exclusively for binary network sockets

(C) `ifstream` is for input reading from files; `ofstream` is for output writing to files

(D) `ifstream` is for output writing; `ofstream` is for input reading

Q.76 8.6 Generic Programming: Class Templates

What is a **Class Template in C++?**

(A) A generic blueprint that allows a class to be parameterized by data types, enabling identical class logic to operate on arbitrary types

(B) A class without any data attributes

(C) A compiled binary dynamic link library (DLL)

(D) An abstract base class containing only private member functions

Q.77 8.1 Computer-Aided Software Engineering: CASE Tools

In Computer-Aided Software Engineering (CASE), what primary functional support is provided by **Code Generation CASE Tools?**

(A) Compiling assembly language into silicon photomasks

(B) Automatically conducting end-user requirement interviews

(C) Writing marketing brochures and software sales contracts

(D) Automated conversion and generation of source code skeletons directly from high-level UML design diagrams, database schemas, and data flow models

Q.78 8.6 Implementation: C Operator Precedence

What is the terminal output of the following C program segment demonstrating prefix and postfix decrement operators?

```
 int i = 5;
int a = --i + i--;
printf("%d %d", a, i);
```

(A) `8 4`

(B) `8 3`

(C) `7 4`

(D) `7 3`

Q.79 8.2 Software Design: Cohesion

Which software design attribute measures the degree of functional strength and focused singleness of purpose within a single software module?

(A) Inheritance Multiplicity

(B) Coupling

(C) Cohesion

(D) Cyclomatic Complexity

Q.80 8.3 Software Testing: Black-Box Techniques

In black-box software testing, dividing the input domain into groups of valid and invalid data values such that testing one representative value from each group is presumed to cover all values in that group is called:

(A) Basis Path Testing

(B) Equivalence Partitioning

(C) Mutation Testing

(D) Stress Testing

SECTION IX: ARTIFICIAL INTELLIGENCE AND NEURAL NETWORKS

Questions 81 – 90 (10 Marks)

Q.81 9.1 AI Foundations & Intelligent Agents

In Artificial Intelligence, an autonomous Intelligent Agent is fundamentally defined by Russell and Norvig as consisting of which two components?

(A) Hardware Sensors + Actuators only

(B) Architecture (physical computing device) + Agent Program (function mapping percepts to actions)

(C) Relational Database + SQL Engine

(D) Inference Engine + Natural Language Parser

Q.82 9.2 Uninformed Search: Breadth-First Search

Which uninformed (blind) search algorithm expands all nodes at the current depth level before exploring nodes at the next deeper level, guaranteeing an optimal (shortest) path for unit step costs?

(A) Depth-Limited Search (DLS)

(B) Hill Climbing

(C) Depth-First Search (DFS)

(D) Breadth-First Search (BFS)

Q.83 9.2 Informed Search: A* Evaluation Function

In the A* heuristic search evaluation function $f(n) = g(n) + h(n)$, what does component $h(n)$ represent?

(A) An estimated heuristic cost to reach the goal node from current node n

(B) The branching factor of the search tree

(C) The exact cost incurred along the path from the start node to current node n

(D) The total number of nodes expanded so far

Q.84 9.2 Adversarial Search: Alpha-Beta Pruning

In the Minimax game-playing algorithm, how does Alpha-Beta pruning optimize search performance without changing the final minimax decision?

(A) By discarding all branches that have evaluation scores below zero

(B) By randomly skipping move evaluations during time constraints

(C) By pruning subtrees that are mathematically proven to be inferior to an already explored option, reducing best-case time complexity from $O(b^d)$ to $O(b^{d/2})$

(D) By restricting tree depth strictly to 2 plies

Q.85 9.3 Knowledge Representation: First-Order Logic

Which formal logic system extends Propositional Logic by incorporating objects, properties, relations between objects, and existential/universal quantifiers ($\exists, \forall$)?

(A) Fuzzy Multi-Valued Logic

(B) Boolean Switching Algebra

(C) Propositional Logic

(D) First-Order Predicate Logic (FOPL)

Q.86 9.5 Machine Learning: Learning Paradigms

In machine learning classification, training an algorithm on a dataset containing input features along with corresponding ground-truth target output labels is classified as:

(A) Supervised Learning

(B) Hebbian Learning

(C) Unsupervised Learning

(D) Reinforcement Learning

Q.87 9.3 Probabilistic Reasoning: Bayes' Rule

In artificial intelligence reasoning under uncertainty, which fundamental theorem calculates the posterior probability of a hypothesis H given observed evidence E via $P(H|E) = \frac{P(E|H)P(H)}{P(E)}$?

(A) Central Limit Theorem
(B) De Morgan's Theorem
(C) Bayes' Theorem
(D) Nyquist-Shannon Theorem

Q.88 9.6 Neural Networks: Perceptron Limitations

In 1969, Marvin Minsky and Seymour Papert proved that a single-layer artificial perceptron with a threshold activation function cannot solve which classic logical problem?

(A) Logical OR
(B) Logical NOT
(C) Logical AND
(D) Logical XOR (Exclusive-OR)

Q.89 9.6 Neural Networks: Activation Functions

Which mathematical activation function standardly maps any real-valued input $x \in (-\infty, +\infty)$ into a continuous smooth probability-like output strictly in the range $(0, 1)$ via $f(x) = \frac{1}{1+e^{-x}}$?

(A) Binary Step Function
(B) Sigmoid (Logistic) Function
(C) Rectified Linear Unit (ReLU)
(D) Hyperbolic Tangent (Tanh)

Q.90 9.6 Neural Networks: Backpropagation Algorithm

The **Backpropagation Algorithm used to train multi-layer feedforward neural networks minimizes prediction error using which mathematical optimization method?**

(A) Gradient Descent applying the calculus Chain Rule backwards from output to input layers
(B) Genetic Crossover and Mutation Selection
(C) Simplex Linear Programming Optimization
(D) Branch and Bound Integer Search

SECTION X: PROJECT PLANNING, DESIGN AND IMPLEMENTATION

Questions 91 – 100 (10 Marks)

Q.91 10.1 Engineering Drawings: Standard Sheet Sizes

According to ISO 216 standard technical drafting conventions, what are the standard trimmed dimensions (width $\times$ length in mm) of an **A3 drawing sheet?**

(A) 210×297 mm
(B) 420×594 mm
(C) 297×420 mm
(D) 594×841 mm

Q.92 10.2 Engineering Economics: Depreciation

Which method of charging depreciation of an engineering asset charges an EQUAL fixed amount of depreciation expense in each year of its useful economic life?

(A) Straight-Line Method
(B) Sinking Fund Method
(C) Sum-of-the-Years'-Digits Method
(D) Declining Balance Method

Q.93 10.3 Project Planning: Resource Scheduling

The project management technique of shifting non-critical activities within their float limits to even out resource demand WITHOUT extending the total project completion duration is called:

(A) Project Crashing
(B) Resource Smoothing
(C) Resource Levelling
(D) Fast Tracking

Q.94 10.4 Project Management: Project Financing

The formal financial process of estimating, assembling, and raising the required capital funds from various sources (equity, commercial loans, bonds) to implement an engineering venture is known as:

(A) Project Accounting
(B) Tender Bid Evaluation
(C) Value Engineering
(D) Project Financing

Q.95 10.5 Professional Practice & Ethics: Society

In professional engineering practice and corporate governance, establishing transparent ethical codes and adherence to regulatory mandates serves primarily to:

(A) Prevent government bodies from auditing project accounting books
(B) Grant monopoly commercial power to established legacy contractors
(C) Safeguard public health, life safety, and societal welfare while ensuring professional accountability
(D) Maximize short-term corporate executive bonuses

Q.96 10.6 Regulatory Body: Nepal Engineering Council Act

According to the Nepal Engineering Council Act, 2055 (and its Amendment 2079), all academic engineering institutions operating within Nepal must be:

(A) Officially recognized and registered with the Nepal Engineering Council
(B) Exempt from institutional quality accreditation
(C) Privately funded and autonomous from government oversight
(D) Affiliated exclusively with foreign technical universities

Q.97 10.2 Engineering Economics: Interest Rates

If a bank offers a nominal annual interest rate of 12% compounded monthly, what is the effective monthly interest rate?

(A) 1.2%
(B) 6.0%
(C) 12.68%
(D) 1.0%

Q.98 10.3 Project Planning: Critical Path Method

In Critical Path Method (CPM) project network scheduling, the **Critical Path is defined as:**

(A) The path that incurs the least financial budget expenditure
(B) The longest continuous sequence of dependent activities having zero total float, which dictates the minimum possible time required to complete the project
(C) A path composed exclusively of dummy activities
(D) The path through the network with the shortest calendar duration and maximum total float

Q.99 10.6 Regulatory Framework: Registration Categories

Under the Nepal Engineering Council (NEC) Act 2055 and its regulatory rules, how many statutory categories of engineers are recognized for registration?

(A) A single unified registration category without distinction
(B) 2 categories (General Engineer and Graduate Engineer)
(C) 4 categories (Assistant, Associate, Executive, and Fellow)
(D) 3 categories (General Registered Engineer, Professional Engineer, and Foreign Engineer)

Q.100 10.4 Project Procurement: Performance Security

Under the Public Procurement Act, 2063 and Public Procurement Rules, 2064 of Nepal, what security deposit is standardly required to be furnished by the winning bidder upon signing the formal contract?

(A) Bid Security (Earnest Money Deposit) of 2% to 3%

(B) Performance Security of 5% of the total contract price

(C) Retention Money of 15% upfront

(D) Mobilization Advance Guarantee of 50%